CONTACT EFFECTS ON HF LOSS OF CPW HIGH RESISTIVITY SILICON LINES

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ABSTRACT

This paper shows that the HF losses of CPW lines realized on 5-10 KΩ.cm HRS (High Resistivity Silicon) substrates are strongly affected by the derivative of the I-V curves, ie. HF losses are higher where the I-V characteristic changes most rapidly. As a result the excess HF loss due to choice of quiescent bias voltage can be as high as 0.3-0.4 dB/cm. The implication of the effect is that by proper dc biasing of a CPW line on HRS substrate minimum HF loss can be achieved. This is of importance when active devices are to be biased through line interconnects.

Introduction

The HF losses of CPW (coplanar waveguide) lines on HRS (High Resistivity Silicon) as a function of frequency and temperature have been previously studied in detail[1-4]. However, the I-V characteristics of a CPW line on HRS substrate and its effects on HF loss have not yet been reported in the literature. Results presented here show that the HF losses of CPW lines on 5-10 KΩ.cm HRS substrates are strongly affected by the derivative of the I-V curves obtained due to metal-semiconductor barriers between the gate and ground plates and the silicon material.

Measured and Simulated Results

The CPW transmission line, as shown in Figure 1, is constructed on 635 μm thick 5-10 kΩ.cm high resistivity silicon substrate with <111> crystal orientation. The line dimensions are selected to give a nominal 50 Ω characteristic impedance and to accommodate 200 μm pitch

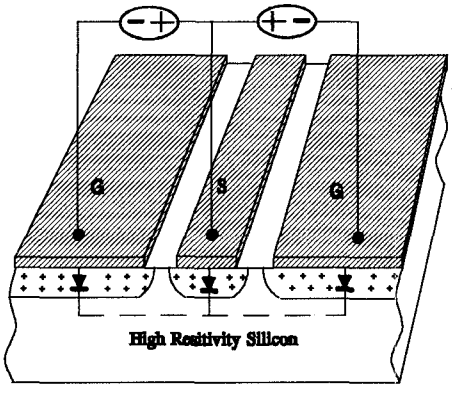

Figure 1 Cross sectional view of the CPW transmission line

GSG CPW probes. The selected line spacing is 40 μm, signal line width is 70 μm, and a physical length 6100 μm is chosen. For an Al CPW line, the 1 μm thickness Al metallization layer is evaporated onto HRS. For a Ti/Au CPW line, A 300 Å Ti thin film layer is evaporated onto HRS and then the Au metallization layer is deposited onto the Ti layer with 0.8 μm thickness.

I-V measurements of CPW lines have been carried out using an HP 4142B Modular DC Source/Monitor and CASCADE wafer probe station. The results are shown in Figure 2 for both Al and Ti/Au CPW lines. The interesting

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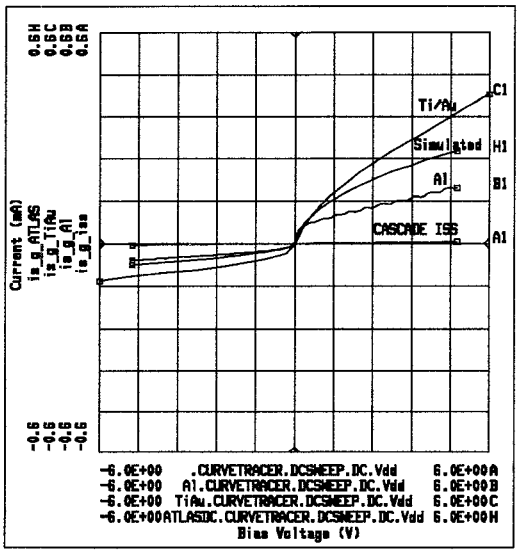

Figure 2 I-V characteristics of CPW lines on 5-10 KΩ.cm HRS substrates

observation from the figure is that current change with bias voltage is nonlinear. This may well be contributed by the existence of metal-semiconductor barriers underneath the gate and ground plates. Theoretically, it should be possible to create an ohmic contact as long as the metal work function is less than semiconductor one. However, for most semiconductors, because of the presence of interface states, ohmic contacts can not be obtained by normal choice of metal work function[5]. It is very likely that when metal is evaporated onto HRS a metal-semiconductor barrier is present leading to a rectifying contact as show in Figure 1. The gate barrier and ground barriers act as two back to back diodes, which gives rise to rapidly changing current around zero bias and smoothly increasing current as the bias voltage is further increased. Figure 2 also shows the simulated I-V characteristics from SILVACO ATLAS II semiconductor simulator, for $4x10^{11}$ N type silicon with a 4.71 V 'effective' work function[6], which qualitively confirms the experimental observations.

The rapid change of current verses voltage contributes to lower dynamic or ac resistance, which implies that HF losses around zero bias will be higher than those at other bias points. This has been confirmed in Figure 3 and 4, where s-parameters are measured for different dc bias levels supplied. Figure 3 shows the HF losses of Al CPW line biased at zero, 0.5 and 5.0 volts, as can be seen the losses for the zero bias condition is consistently about 0.3-0.4 dB/cm higher than that for the 5 volt bias level ranging over the frequency range 1 to 40 GHz. Figure 4 illustrates the HF losses of Ti/Au CPW line for the same dc bias sequence. The higher HF losses exhibited at zero bias through 5 volts bias can be seen, though the differences are smaller than where observed in Figure 3. For Al CPW line, the dynamic or ac resistance,

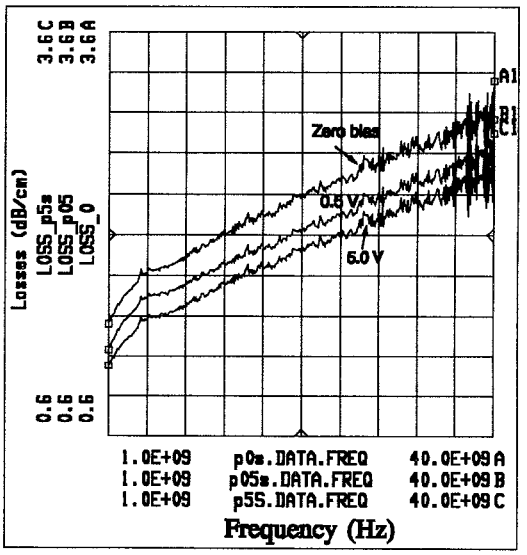

Figure 3 HF losses of an Al CPW line on a 5-10 KΩ.cm HRS substrate at different dc bias points

ie. $\Delta R=\Delta V/\Delta I$, obtained at zero bias is much lower than that at 5.0 volt bias ($\Delta R_{v=0}$= 1604 Ω, $\Delta R_{v=5.0}$= 20408 Ω), hence losses at zero bias are much higher than at 5.0 volt bias. For Ti/Au CPW line, however, the difference of ΔR on

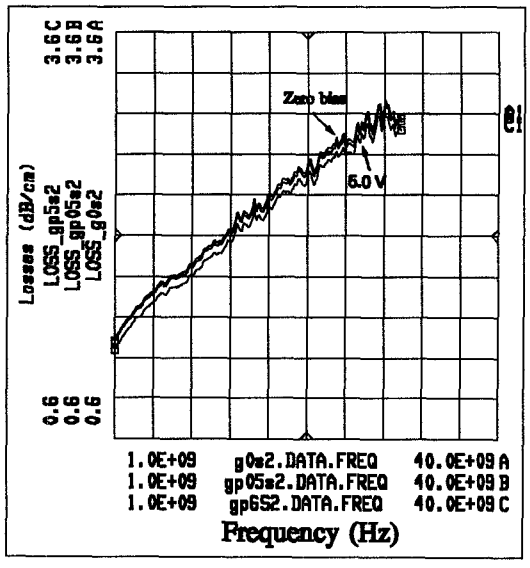

Figure 4 HF losses of a Ti/Au CPW line on a 5-10 kΩ.cm HRS substrate with different bias points

zero and 5.0 volts bias is smaller ($\Delta R_{v=0}$= 6918.5 Ω, $\Delta R_{v=5.0}$= 10655 Ω), consequently, the divergence of the losses at different bias points is smaller. Figure 5 shows the phase of S_{21} from 1 to 40 GHz for the Al CPW line biasing at zero, 0.5 and 5.0 volts, respectively. As we can see the phase is virtually independent of the dc bias. Analysis of these results indicates that by properly biasing a CPW line on a HRS substrate, minimum intrinsic HF losses can be obtained.

An Al slot line ring antenna, as shown in Figure 6, was fabricated on the same wafer as the Al CPW lines. The slot is 63 μm wide and the inner radius of the ring is 3242 μm. The interconnect CPW line has the same geometry as mentioned above. The resonator has been designed to have a fundamental resonant frequency being 8.76 GHz. Table 1 shows $|S_{11}|$ at the fundamental frequency f_o and second harmonic frequency $3f_o$ for a DC bias sequence 0.0, 0.5 and 5.0 volts. It can be seen that the reflection losses are higher around zero bias and lower at higher bias voltage in keeping with the observation reported for the CPW interconnect.

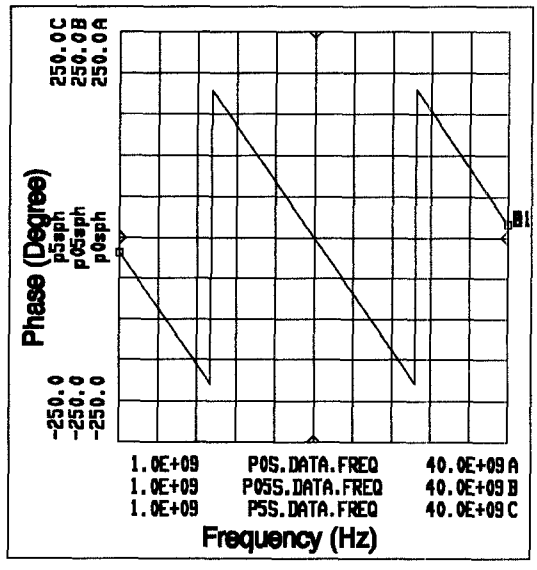

Figure 5 Phases of S_{21} for Al CPW lines on a 5-10 KΩ.cm HRS substrate with different dc bias points

Conclusions

This paper discussed the effect of DC bias on HF losses of CPW lines. It was shown that the lines could be made to have bias dependant loss under DC bias control. A suggested cause of the effect is that a rectifying rather than an ohmic contact is formed at the metal-silicon interface.

Acknowledgement

The authors wish to thank Dr. Raza for constructing the circuits used in this work. This work was funded under Engineering Physical Science and Research Council contract GR/J86544.

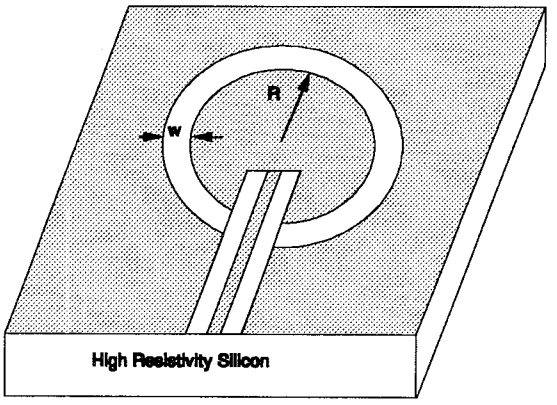

Figure 6 A slot line ring antenna on HRS substrate

Table I Reflection losses of a slot line ring antenna

Bias (V)	ΔR (Ω)	$\|S_{11}\|_{fo}$ (dB)	$\|S_{11}\|_{3fo}$ (Db)
0.0	4080	-37.46	-38.20
0.5	6800	-38.20	-41.41
5.0	17000	-39.66	-46.74

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